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INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
HOANG, PHI	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,172	LIANG ET AL.	
	Examiner	Art Unit	
	PHI HOANG	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7,8,11,12 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8,11,12 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 15 March 2010 have been fully considered but they are not persuasive.

2. With regard to claims 1, 12, and 15, Applicant states, Chandley does not disclose, "…fetching pixels from different segment of the frame buffer during different power states..." However, Chandley (Column 9, lines 17-39) discloses reducing power by not retrieving certain color channels each indicated by an 8-bit value representing 0 to 255. During low power phases, Chandley discloses that any one of the R, G, or B values may not be read out from memory or all three channel values may not be read out from memory. Therefore, since certain channels may not be read out from memory during a lower power phase, Chandley discloses "fetching pixels from different segment of the frame buffer during different power states."

Furthermore, Applicant states, the cited prior art does not disclose "…performing an error diffusion…and diffusing the error to up to two neighboring pixels of the source pixel." However, Long (Paragraph 0011) discloses performing an error diffusion operation on the pixels to reduce a color depth of the pixels, where an error diffusion mask is applied to an image. Chandley (Column 8, lines 32-36) discloses the normal and low power states are independent and switchable from each other by allowing a user to input a command to adjust the power state.

In addition, Zhang was stated by Applicant to not disclose, "for each source pixel of each color plane of the image data, calculating an output value corresponding to a

source pixel value of the source pixel according to a predetermined algorithm, calculating an error between the output value and the source pixel value; and diffusing the error to up to two neighboring pixels of the source pixel." However, Long (Paragraph 0031) discloses converting 8-bit color depth to 6-bit color depth during error diffusion. Zhang (Page 5, paragraph 0060, lines 13-17) is relied upon to disclose "calculating an error between the output value and the source pixel value; and diffusing the error to **up to two** neighboring pixels of the source pixel," where the error of Zhang can be "**diffused to one** or more neighboring pixels." (Emphasis added) Therefore the cited prior discloses, "…performing an error diffusion…and diffusing the error to up to two neighboring pixels of the source pixel."

Furthermore, Applicant states, "…Zhang fails to disclose the specific limitation of arithmetically adding the error diffused from up to two neighboring pixels to an original value of a pixel, and storing a predetermined number of most significant bits (MSBs) of the output value. However, Zhang (Page 6, paragraph 0060) discloses subtracting an error value from a pixel, where subtraction is equivalent to addition with negative numbers. Chandley (Column 10, line 30) is relied upon to disclose storing a predetermined number of most significant bits (in this case 8-bits of a 24-bit word) in order to reduce power consumption. Therefore the cited prior art discloses all limitations of claims 1, 12, and 15.

Since the position of the Examiner on claims 1, 12, and 15 is maintained, the Examiner's position on claims 2, 4, 5, 7, 8, and 11 is also maintained.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 7, 8 11, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashburn et al. (US 2003/0090486 A1) in view of Long (US 2004/0174463 A1) in view of Chandley et al. (US 7,389,432 B2) and further in view of Zhang et al. (US 2006/0077489 A1).

5. Regarding claims 1, 12 and 15, Ashburn discloses storing pixels into a frame (Paragraph 0004) buffer where the frame buffer is divided into addresses of an address space corresponding to rows and columns of the pixel (Paragraph 0007).

Ashburn does not clearly disclose performing an error diffusion operation on the pixels to reduce a color depth of the pixels, including for each source pixel of each color plane of the image data, calculating an output value corresponding to a source pixel value of the source pixel according to a predetermined algorithm, and storing at least a portion of the pixels with reduced color depth in the frame buffer.

Long discloses performing an error diffusion operation on the pixels to reduce a color depth of the pixels for each source pixel of each color plane of the image data (Figure 2), calculating an output value corresponding to a source pixel value of the source pixel according to a predetermined algorithm (Page 3, paragraph 0031) and

storing at least a portion of the pixels with reduced color depth in the frame buffer (Page 1, paragraph 0011).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ashburn to reduce a color depth of pixels to be read by a display device because larger compatibility with various displays can be obtained while attempting to maintain high image detail.

Ashburn in view of Long does not clearly disclose a normal power state and a low power state, where in a low power state, the error diffusion operation is performed on the pixels, wherein the normal and low power states are independent and switchable from each other and not accessing the second segment of the frame buffer during the low power state; during the normal power state, fetching the pixels from the first and second segments of the frame buffer for display; and during the low power state, fetching the pixels with reduced color depth from the first segment of the frame buffer for display without accessing the second segment of the frame buffer; and reducing color bits of each pixel with reduced color depth to fit within the first segment of the frame buffer prior to storing each pixel in the first segment of the frame buffer and storing a predetermined number of most significant bits (MSBs) of the output value in the first segment of the frame buffer.

Chandley discloses switching from a normal power state to an independent low power state (Column 8, lines 32-36) and performing a color depth reduction in the low power state by not reading a number of bits of a pixel from the address space of the frame buffer (Column 10, lines 17-34)

and during the normal power state, fetching the pixels from the first and second segments of the frame buffer for display; (Column 1, lines 40-53 and column 9, lines 6-16)

and during the low power state, fetching the pixels with reduced color depth from the first segment of the frame buffer for display without accessing the second segment of the frame buffer (Column 9, lines 29-39, bits of a color channel are not retrieved);

and reducing color bits of each pixel with reduced color depth to fit within the first segment of the frame buffer prior to storing each pixel in the first segment of the frame buffer (Column 10, lines 17-34, 24 bit reduced to 8 bit)

and storing a predetermined number of most significant bits (MSBs) of the output value in the first segment of the frame buffer (Chandley, column 10, line 30, 8 bits are only used).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ashburn in view of Long to allow a user to switch between power states in a device as disclosed by Chandley because a user can at any time decide on the amount of detail processing desired for display especially when on a limited power supply.

Ashburn in view of Long and further in view of Chandley does not disclose calculating an error between the output value and the source pixel value; and diffusing the error to up to two neighboring pixels of the source pixel and for each pixel of a color plane, and arithmetically adding the error diffused from up to two neighboring pixels to an original value of a pixel.

Zhang discloses calculating an error between the output value and the source pixel value; and diffusing the error to up to two neighboring pixels of the source pixel and for each pixel of a color plane, arithmetically adding the error diffused from up to two neighboring pixels to an original value of a pixel, (Zhang, page 6, paragraph 0060, one or more neighboring pixels).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ashburn in view of Long and further in view of Chandley to incorporate at error into nearby pixels as disclosed by Zhang because the color values of the nearby pixels can be visually compensated for the differences in color value of the source pixel resulting in an improved image.

6. Regarding claim 2, Chandley discloses reducing power to the second segment of the frame buffer during the low power state (Column 9, lines 29-39, a color channel is shut off with a value of 0 at different points in time to reduce power consumption).

7. Regarding claim 4, Chandley discloses the first segment is a most significant device (MSD) of the frame buffer and the second segment is a least significant device (LSD) of the frame buffer (Column 9, lines 29-39, 16 bits of a pixel during a refresh time are used as the "MSD" while the other 8 unused bits are the "LSD" of a 24 bit color pixel).

8. Regarding claim 5, Chandley discloses during the low power state, pixels with reduced color depth are used as data associated with the MSD for display (Column 9, lines 32-33, two channels for MSD) while a predetermined value is used as data

associated with the LSD for display without accessing the LSD of the frame buffer (A 0 is used for one color channel to reduce power consumption during a refresh).

9. Regarding claim 7, Chandley (Column 9, lines 40-44) in view of Zhang (Page 5, paragraph 0054, lines 5-13) discloses the up to two neighboring pixels are a right pixel and a bottom pixel of the source pixel.

10. Regarding claim 8, Zhang discloses diffusing the error to up to two neighboring pixels comprises adjusting pixel values of the up to two neighboring pixels with at least a portion of the error, wherein the portion of the error diffused to the neighboring pixel in an identical row is temporarily stored in a register and a portion of the error diffused to the neighboring pixel in a next row is temporarily stored in a line buffer (Page 6, paragraph 0060, location of storage for pixel data is a design choice and does not affect the end result).

11. Regarding claim 11, Chandley discloses the error diffusion operation is performed by an encoder implemented within at least one of software, a display controller, and a chipset of a data processing system (Column 7, lines 31-38).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHI HOANG whose telephone number is 571-270-3417. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phi Hoang/
Examiner, Art Unit 2628
June 17, 2010

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628